Amendments to the Claims:

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor device, comprising:

a first portion and a second portion;

~~a plurality~~first and second groups of landing pads formed in the first and second portions, respectively, of the semiconductor device, the landing pads being sized and shaped to be used with bonding pads, the first group of the landing pads being different than the second group of the landing pads;

a plurality of the bonding pads formed over [[a]]the first group~~portion~~ of the landing pads and not formed over the second group of the landing pads; and

a power supply line formed over [[a]]the second group~~portion~~ of the landing pads and not formed over the first group of the landing pads.

2. (Original) The semiconductor device of claim 1, wherein the bonding pads are formed in a first direction on the semiconductor device and the power supply line is formed in a second direction.

3. (Original) The semiconductor device of claim 2, wherein the first and second directions are perpendicular.

4. (Original) The semiconductor device of claim 2, wherein the first and second directions are different.

5. (Original) The semiconductor device of claim 1, wherein the power supply line is a power voltage supply line.

6. (Original) The semiconductor device of claim 1, wherein the power supply line is a ground line.

7. (Currently Amended) The semiconductor device of claim 1, further comprising a second power supply line formed over the second ~~portion~~group of the landing pads.

8. (Original) The semiconductor device of claim 7, wherein one of the first and second power supply lines is one of a power voltage line and a ground line.

9. (Original) The semiconductor device of claim 8, wherein the other of the first and second power supply lines is the other of the power voltage line and the ground line.

10. (Original) The semiconductor device of claim 1, wherein each of the landing pads comprises a conductive layer.

11. (Original) The semiconductor device of claim 1, wherein each of the landing pads comprises a metal layer.

12. (Original) The semiconductor device of claim 1, wherein each of the landing pads comprises a polysilicon layer.

13. (Original) The semiconductor device of claim 1, wherein each of the landing pads comprises a gate polysilicon layer, a plate polysilicon layer and a metal layer.

14. (Original) The semiconductor device of claim 1, wherein the semiconductor device is a memory circuit.

15. (Original) The semiconductor device of claim 1, wherein the semiconductor device comprises a plurality of memory blocks defining a center region of the semiconductor device between memory blocks and an edge region at an edge of the memory blocks.

16. (Original) The semiconductor device of claim 15, wherein the landing pads are formed in both the center region and the edge region.

17. (Currently Amended) The semiconductor device of claim [[1]]15, wherein one of the bonding pads and the power line is formed in one of the center region and the edge region, and the other of the bonding pads and the power line is formed in the other of the center region and the edge region.

18. (Original) The semiconductor device of claim 1, wherein the device can be used in one of a board on chip (BOC) configuration and a multichip package (MCP) configuration.

19. (Currently Amended) A semiconductor device, comprising:

a plurality of circuit blocks defining a center region between circuit blocks and an edge region at an edge of the circuit blocks;

a first plurality of landing pads formed in the center region and a second plurality of landing pads formed in the edge region, the landing pads being sized and shaped to be used with bonding pads;

a plurality of bonding pads formed over one of [[(i)]] the first plurality of landing pads and [[(ii)]] the second plurality of landing pads and not formed over the other of the first plurality of landing pads and the second plurality of landing pads; and

a power supply line formed over the other of the first plurality of landing pads and the second plurality of landing pads and not formed over the one of the first plurality of landing pads and the second plurality of landing pads.

20. (Original) The semiconductor device of claim 19, wherein the circuit blocks are memory blocks.

21. (Original) The semiconductor device of claim 19, wherein the bonding pads are formed in the center region, and the power supply line is formed in the edge region.

22. (Withdrawn) The semiconductor device of claim 19, wherein the power supply line is formed in the center region, and the bonding pads are formed in the edge region.

23. (Original) The semiconductor device of claim 19, wherein the bonding pads are formed in a first direction on the semiconductor device and the power supply line is formed in a second direction.

24. (Original) The semiconductor device of claim 19, wherein the power supply line is a power voltage supply line.

25. (Original) The semiconductor device of claim 19, wherein the power supply line is a ground line.

26. (Original) The semiconductor device of claim 19, further comprising a second power supply line formed over the other of the first plurality of landing pads and the second plurality of landing pads.

27. (Original) The semiconductor device of claim 26, wherein one of the first and second power supply lines is one of a power voltage line and a ground line.

28. (Original) The semiconductor device of claim 27, wherein the other of the first and second power supply lines in the other of the power voltage line and the ground line.

29. (Original) The semiconductor device of claim 19, wherein each of the landing pads comprises a conductive layer.

30. (Original) The semiconductor device of claim 19, wherein each of the landing pads comprises a metal layer.

31. (Original) The semiconductor device of claim 19, wherein each of the landing pads comprises a polysilicon layer.

32. (Original) The semiconductor device of claim 19, wherein each of the landing pads comprises a gate polysilicon layer, a plate polysilicon layer and a metal layer.

33. (Original) The semiconductor device of claim 19, wherein the device can be used in one of a board on chip (BOC) configuration and a multichip package (MCP) configuration.

34. - 48. (Cancelled)

49. (New) The semiconductor device of claim 15, wherein the first portion of the semiconductor device comprises the center region, and the second portion of the semiconductor device comprises the edge region.

50. (New) The semiconductor device of claim 15, wherein the first portion of the semiconductor device comprises the edge region, and the second portion of the semiconductor device comprises the center region.